WHAT IS CLAIMED IS:

1. A thin film transistor array substrate comprising:

an insulating substrate;

a first signal line formed on the insulating substrate;

a first insulating layer formed on the first signal line;

a second signal line formed on the first insulating layer while crossing over the first signal line;

a thin film transistor connected to the first and the second signal lines;

a second insulating layer formed on the thin film transistor, the second insulating layer having dielectric constant about 4.0 or less, and the second insulating layer having a first contact hole exposing a predetermined electrode of the thin film transistor; and

a first pixel electrode formed on the second insulating layer while being connected to the predetermined electrode of the thin film transistor through the first contact hole.

2. The thin film transistor array substrate of claim 1, wherein the first insulating layer includes a top layer and a bottom layer, the bottom layer having dielectric constant about 4 or less, and the top layer being a silicon nitride layer.

3. The thin film transistor array substrate of claim 1, wherein the first pixel electrode is formed with an electrically conductive and optically opaque material.

4. The thin film transistor array substrate of claim 3, wherein the second insulating layer has a pattern of protrusion and depression.

5. The thin film transistor array substrate of claim 1, further comprising:

a third insulating layer formed on the first pixel electrode having dielectric constant about 4.0 or less, the third insulating layer having a second contact hole exposing a predetermined portion of the first pixel electrode; and

a second pixel electrode formed on the third insulating layer, the third insulating layer is formed with an electrically conductive and optically opaque material while being connected to the predetermined portion of the first pixel electrode through the second contact hole;

wherein the first pixel electrode is formed with an optically transparent and electrically conductive material, and the second pixel electrode has a predetermined opening portion capable of passing light transmitted through the first pixel electrode.

6. The thin film transistor array substrate of claim 1, wherein the second insulating layer is formed with an a-Si:C:O layer or an a-Si:O:F layer.

7. The thin film transistor array substrate of claim 6, wherein the a-Si:C:O layer is formed through plasma enhanced chemical vapor deposition (PECVD) using a gaseous material selected from the group consisting of $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$, and $Si(C_2H_5O)_4$ and an oxide agent of N_2O or O_2.

8. The thin film transistor array substrate of claim 6, wherein the a-Si:O:F layer is formed through plasma enhanced chemical vapor deposition (PECVD) by introducing a material selected from the group consisting of SiH_4 and SiF_4 with CF_4 and O_2 added.

9. The thin film transistor array substrate of claim 1, wherein the second insulating layer has a dielectric constant of about 2 to about 4.

10. The thin film transistor array substrate of claim 1, wherein the first signal line includes a first alloy layer and a second alloy layer, the first alloy layer is a Cr alloy layer or a Mo alloy layer and the second alloy layer is a Al alloy layer or a Ag alloy layer.

11. The thin film transistor array substrate of claim 1, wherein the first pixel electrode is made of an optically transparent and electrically conductive material.

12. The thin film transistor array substrate of claim 11, wherein the transparent conductive material is indium tin oxide (ITO) or indium zinc oxide (IZO).

13. A thin film transistor array substrate comprising:

a data line assembly formed on an insulating substrate, the data line assembly including data lines;

a plurality of color filters formed on the insulating substrate, each of the plurality of color filters including a red color filter, a green color filter, and a blue color filter;

a buffer layer formed on the data line assembly and the color filters, the buffer layer having a first contact hole exposing a predetermined portion of the data line assembly;

a gate line assembly formed on the buffer layer, the gate line assembly including gate lines crossing over the data lines while defining pixel regions, and gate electrodes connected to the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a second contact hole partially exposing the first contact hole;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes; and

a pixel line assembly including pixel electrodes, drain electrodes and source electrodes, the source electrodes connected to the data lines through the first and the second contact holes, the pixel line assembly having a portion witch contacts the semiconductor pattern, the drain electrodes facing the source electrodes over the semiconductor pattern, and the pixel electrodes connected to the drain electrodes.

14. The thin film transistor array substrate of claim 13, wherein the semiconductor pattern includes a first amorphous silicon layer with a predetermined band gap, and a second amorphous silicon layer with a band gap lower than the band gap of the first amorphous silicon layer.

15. The thin film transistor array substrate of claim 14, further comprising light absorption members formed at the same plane as the data lines with the same

material as the data lines while being placed corresponding to the semiconductor pattern.

16. The thin film transistor array substrate of claim 15, wherein the light absorption members are extended toward the gate lines.

17. The thin film transistor array substrate of claim 13, wherein the buffer layer has dielectric constant about 4.0 or less.

18. The thin film transistor array substrate of claim 17, wherein the buffer layer has a dielectric constant of about 2 to about 4.

19. The thin film transistor array substrate of claim 13, wherein the buffer layer is formed with an a-Si:C:O layer or an a-Si:O:F layer.

20. A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly including gate lines, gate electrodes, and gate pads;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having contact holes exposing the gate pads;

a semiconductor pattern formed on the gate insulating layer;

an ohmic contact pattern formed on the semiconductor pattern;

a data line assembly formed on the ohmic contact pattern while having substantially the same shape as the ohmic contact pattern, the data line assembly including source electrodes, drain electrodes, data lines, and data pads;

a passivation pattern formed on the data line assembly having dielectric constant about 4.0 or less, the passivation pattern having contact holes exposing the gate pads, the data pads, and the drain electrodes; and

a transparent electrode pattern electrically connected to the gate pads, the data pads, and the drain electrodes.

21. The thin film transistor array substrate of claim 20, further comprising:

storage capacitor lines formed at the same plane as the gate line assembly;

a storage capacitor semiconductor pattern overlapped with the storage capacitor lines while being placed at the same plane as the semiconductor pattern;

a storage capacitor ohmic contact pattern formed on the storage capacitor semiconductor pattern while having substantially the same outline as the storage capacitor semiconductor pattern; and

a storage capacitor conductive pattern formed on the storage capacitor ohmic contact pattern while having substantially the same outline as the storage capacitor semiconductor pattern,

wherein the storage capacitor conductive pattern is partially connected to the transparent electrode pattern.

22. The thin film transistor array substrate of claim 20, wherein the passivation pattern has a dielectric constant of about 2 to about 4.

23. The thin film transistor array substrate of claim 20, wherein the passivation pattern is formed with an a-Si:C:O layer or an a-Si:O:F layer.

24. A method of fabricating a thin film transistor array substrate, the method comprising the steps of:

forming a gate line assembly, the gate line assembly including gate lines, gate electrodes connected to the gate lines, and gate pads connected to the gate lines;

forming a gate insulating layer;

forming a semiconductor layer;

forming a data line assembly through depositing and patterning a conductive layer, the data line assembly including data lines crossing over the gate lines, data pads connected to the data lines, source electrodes connected to the data lines while being placed adjacent to the gate electrodes, and drain electrodes facing the source electrodes around the gate electrodes;

forming a passivation layer having a dielectric constant about 4.0 or less;

patterning the gate insulating layer together with the passivation layer to thereby form contact holes exposing the gate pads, the data pads, and the drain electrodes; and

depositing and patterning a transparent conductive layer to thereby form subsidiary gate pads connected to the gate pads, subsidiary data pads connected to the data pads, and pixel electrodes connected to the drain electrodes.

25. The method of claim 24, wherein the passivation layer is formed through PECVD using a gaseous material selected from the group consisting of $SiH(CH_3)_3$, $SiO_2(CH_3)_4$ and $(SiH)_4O_4(CH_3)_4$ and an oxide agent of N_2O or O_2.

26. The method of claim 24, wherein the passivation layer is formed through PECVD using a gaseous material selected from the group consisting of SiH_4 and SiF_4 with CF_4 and O_2 added.

27. The method of claim 24, wherein the data line assembly and the semiconductor layer are formed through photolithography using a photoresist pattern with a first portion having a predetermined thickness, a second portion having a thickness larger than the thickness of the first portion, and a third portion having a thickness smaller than the thickness of the first portion.

28. The method of claim 27, wherein the first photoresist pattern portion is placed between the source and the drain electrodes, and the second photoresist pattern portion is placed over the data line assembly.

29. The method of claim 24, wherein the step of forming the gate insulating layer comprises the sub-steps of first depositing a CVD layer having dielectric constant about 4.0 or less, and second depositing a silicon nitride layer, the first and second sub-steps being performed in a vacuum state.

30. A method of fabricating a thin film transistor array substrate, the method comprising the steps of:

(a) forming a data line assembly on a substrate, the data line assembly including data lines;

(b) forming color filters of red, green, and blue on the substrate;

(c) forming a buffer layer having dielectric constant about 4.0 or less such that the buffer layer covers the data line assembly and the color filters;

(d) forming a gate line assembly on the insulating layer, the gate line assembly including gate lines and gate electrodes;

(e) forming a gate insulating layer such that the gate insulating layer covers the gate line assembly;

(f) forming an ohmic contact pattern and a semiconductor pattern on the gate insulating layer while forming first contact holes at the gate insulating layer and the buffer layer such that the contact holes partially expose the data lines;

(g) forming a pixel line assembly, the pixel line assembly including source and drain electrodes formed on the ohmic contact pattern at the same plane while being separated from each other, and pixel electrodes connected to the drain electrodes; and

(h) dividing the ohmic contact pattern into two pattern parts through removing the portions of the ohmic contact pattern exposed between the source and the drain electrodes.

31. The method of claim 30, wherein the (f) step comprises the sub-steps

of:

sequentially depositing an amorphous silicon layer and an impurities-doped amorphous silicon layer onto the gate insulating layer;

forming a photoresist pattern such that the photoresist pattern has a first portion covering a predetermined area of the gate electrode with a predetermined thickness, and a second portion covering the remaining area except for the regions of first contact holes to be formed later with a thickness smaller than the thickness of the first portion;

etching the impurities-doped amorphous silicon layer, the amorphous silicon layer, the gate insulating layer and the buffer layer using the first and second portions of the photoresist pattern as a mask to thereby form the first contact holes;

removing the second portion of the photoresist pattern;

etching the impurities-doped amorphous silicon layer and the amorphous silicon layer using the first portion of the photoresist pattern as a mask to thereby form the semiconductor pattern and the ohmic contact pattern; and

removing the first portion of the photoresist pattern.

32. The method of claim 30, wherein the buffer layer has a dielectric constant of about 2 to about 4.